REMARKS

This amendment is being filed in response to the Office Action having a mailing date of August 26, 2005. Claims 4, 6, 8-11, 13-16, 20, 22, 24, 26-29, and 31-35 are amended as shown. Claims 1-3, 7, 12, 17-19, 25, and 30 are canceled herein without prejudice. Claims 37-54 are added. No new matter has been added. With this amendement, claims 4-6, 8-11, 13-16, 20-24, 26-29, 31-54 are pending in the application.

I. Informal Matters

In the Office Action, the Examiner objected to the specification because of some informalities. The specification is amended as shown to address these informalities.

The Examiner further objected to claim 1 because of some minor informalities. These informalities have been addressed in newly independent claim 13.

II. Allowable Subject Matter

In the Office Action, the Examiner objected to claims 5, 8-11, 13-16, 23-24, 26-29, and 31-33 as being dependent upon a rejected base claim, but indicated that such objected claims would be allowable if rewritten in independent form. The applicants thank the Examiner for this indication of allowable subject matter.

Accordingly, claim 13 has been rewritten to include recitations of its former (and now canceled) base claims 1, 7, and 12. Newly independent claim 13 is now allowable. The claims that previously depended upon the canceled claim(s) are amended to be dependent upon newly independent claim 13, amended to make their recitations consistent with newly independent claim 13, and/or otherwise amended so as to be placed in proper form. These dependent claims are now allowable as well.

Dependent claim 31 has been rewritten in independent form to include recitations of its former (and now canceled) base claims 19, 25, and 30. Newly independent claim 31 is now allowable. The claims that previously depended upon these canceled claim(s) are amended to be dependent upon newly independent claim 31, amended to make their recitations consistent with newly independent claim 31, and/or otherwise amended so as to be placed in proper form. These dependent claims are now allowable as well.

New independent claim 37 is directed to a universal asynchronous receiver transceiver circuit and contains recitations that generally parallel those of allowable claim 13. Thus, independent claim 37 is allowable based on these recitations. Independent claim 37 further specifies an oversampling clock signal and a bit clock signal having a frequency that is equal to the frequency of the oversampling clock signal divided by an integer N, while its dependent claim 38 recites that the reference integer Ni is equal to the integer N. As will be explained later below, these are features that are not disclosed, taught, or suggested by any of the references, whether singly or in combination, and therefore, claims 37-38 are further allowable.

III. Discussion of the References in View of the Applicants' Embodiments

In the Office Action, the Examiner rejected claims 1-4, 6-7, 12, 17-22, 25, 30, and 34-36 under 35 U.S.C. § 102(b) as being anticipated by Akiyama (U.S. Patent No. 5,808,493). For the reasons set forth below, the applicants kindly request the Examiner to reconsider.

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

An embodiment of the present applicants relates to a programmable clock generator designed to supply, from an initial signal (*e.g.*, a primary clock signal), a divided signal (*e.g.*, a first clock signal) having a frequency that is equal to the frequency of the initial clock signal divided by a decimal set point M. The decimal set point M of one embodiment comprises a whole part M1 and a decimal part M2.

According to one embodiment, the period of the pulses of the divided signal is pulse width modulated so that the average duration of Ni successive pulses is substantially equal to M*Ni times the period of the initial signal, with Ni being a reference number for the modulation of the period of the pulses of the divided signal. Such a modulation is carried out by dividing the frequency of the initial signal by the whole part M1 of the decimal set point and modulating the value of M1 by discrete values among Ni samples of the first clock signal.

According to a feature of one embodiment, the clock divider is used in a Universal Asynchronous Receiver Transceiver (UART) to produce an accurate oversampling clock signal and an accurate bit clock signal from the oversampling clock signal. That is, in a UART system, a second clock signal is generated that has a frequency equal to the frequency of the first clock signal divided by the number N, which in one embodiment is equal to the number Ni of samples used to implement the pulse width modulated division. For example, Figure 6 and the accompanying description of the present application disclose a signal Hb (*e.g.*, the second clock signal) that is the bit clock signal of the UART, and a signal Hs (*e.g.*, the first clock signal) that is the oversampling clock signal of the UART.

Akiyama does not disclose, teach, or suggest the features provided by the present applicants' embodiments. Akiyama is directed towards a frequency divider 6 used in a phase lock loop (PLL) to divide the output frequency Fout of the PLL before re-injecting Fout in the feedback loop of the PLL. The frequency divider 6 of Akiyama is controlled by an arithmetic circuit 21 that divides Fout by a set point I.J comprising a whole part I and a decimal part J.

The arithmetic unit 21 comprises several cascade-connected cumulative adders. *See, e.g.*, column 9, lines 7-9 of Akiyama. The arithmetic unit 21 of Akiyama therefore appears to perform modulation among a continuum of values with a permanent correction of the integer I, and does not appear to disclose, teach, or suggest the feature of the present applicants' embodiment that modulates the duration of the period of the divided signal so that the duration of Ni successive pulses of the divided signal is substantially equal to M*Ni times the period of the initial signal. For example and in contrast to Akiyama, Figure 6 of the present application shows a circuit MODCT that uses a multiplexer to modify cyclically the division of a set point MY of the counter DIVI during a period of time corresponding to Ni successive pulses.

Other differences from Akiyama can be noted. For example, Akiyama does not involve a UART system, and in particular a UART system that has an oversampling signal and a bit clock signal having a frequency equal to the frequency of the oversampling clock signal.

Instead Akiyama relates to a PLL circuit with no suggestion or motivation to use such a PLL circuit in a UART system as disclosed by the present applicants, in which a divider is used to precisely adjust the oversampling clock signal Hs and the bit clock signal Hb with a decimal divider M comprising the figures after the decimal point.

Akiyama also describes a conventional circuit with reference to his Figure 3A, and further states that the circuit is disclosed by Kingsford-Smith (U.S. Patent No. 3,928,813). *See, e.g.*, column 1, lines 60-65 and Figure 3A of Akiyama. However, a closer reading of Kingsford-Smith reveals that this reference does not cure the deficiencies of Akiyama.

More specifically, Kingsford-Smith does not disclose, teach, or suggest generation of a second clock signal having a frequency equal to the frequency of the first clock signal divided by a number N, which is equal to the number Ni of samples used to implement the pulse width modulated division. As with Akiyma, Kingsford-Smith generally discloses a frequency divider 15 embedded in a feedback loop of a PLL and is silent as to the other features disclosed by the present applicants, including use of an oversampling signal in a UART and a bit clock signal having a frequency equal to the frequency of the oversampling signal divided by an integer N.

IV. Discussion of the Applicants' Other Claims

New independent claim 39 recites a -- universal asynchronous receiver transceiver circuit--, a generator to generate an --oversampling signal--, and --a duration of Ni successive pulses of the oversampling clock signal is substantially equal to M*Ni times a period of the primary clock signal--. As explained above, these features are not disclosed, taught, or suggested by Akiyama and Kingsford-Smith, whether singly or in combination. Accordingly, new independent claim 39 is allowable.

New independent claim 39 further recites --a bit clock signal having a frequency equal to the frequency of the oversampling clock signal divided by an integer N--. Again, this feature is not disclosed, taught, or suggested by the references. Accordingly, new independent claim 39 is further allowable.

New dependent claim 40 recites that --the reference integer Ni used for the modulation of the period of the pulses of the oversampling clock signal is equal to the integer N used to produce the bit clock signal from the oversampling clock signal--. As explained above, no such feature is found in the references. Therefore, claim 40 is allowable.

Other distinctive features are found in the other new dependent claims. For example, claim 50 recites subject matter that the Examiner previously deemed to be distinctive over the prior art. As another example, new claim 54 recites an oversampling register driven by the oversampling clock signal. The register 39 of Figure 12 of Akiyama is described as a "common register" on column 16, lines 31-32, and there is nothing disclosed, taught, or suggested that the register 39 is an --oversampling register-- that is --driven by the oversampling clock signal--.

V. Supplemental Information Disclosure Statement

A Supplemental Information Disclosure Statement (IDS), form PTO-1449, and the requisite certification is being submitted along with this amendment. This Supplemental IDS is being filed so that Kingsford-Smith can be officially placed on record. It is kindly requested that the Examiner return an initialed copy of the form PTO-1449 along with the next communication to confirm that Kingsford-Smith has been considered and will be listed as a cited reference on the front page of the issued patent.

VI. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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